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CIRCUIT AND METHOD FOR PROVIDING AUTOMATIC ADAPTATION TO FREQUENCY OFFSETS IN HIGH SPEED SERIAL LINKS

FIELD OF THE INVENTION

The present invention relates to providing automatic adaptation to frequency offsets in high speed serial links.

BACKGROUND OF THE INVENTION

The ability to perform and achieve high speed transmissions of digital data has become expected in today's computing environment. In most cases, the transmission of digital data over longer distances is accomplished by sending the data in a high-speed serial format (i.e., one single bit after another) over a communication link designed to handle computer communications. In this fashion, data can be transferred from one computer system to another, even if the computer systems are geographically remote.

In order for high-speed serial transmission to occur, the digital data signal from inside the computer must be transformed from the parallel format into a serial format prior to transmission of the data over the serial communication link. This transformation is generally accomplished by processing the computer's internal data signal through a piece of computer equipment known as a serial link transmitter or "serializer." The function of the serializer is to receive a parallel data stream as input and, by manipulating the parallel data stream, output a serial form of the data capable of high-speed transmission over a suitable communication link. Once the serialized data has arrived at the desired destination, a piece of computer equipment known as a "deserializer" is employed to convert the incoming data from the serial format to a parallel format for use within the destination computer system.

For high speed serializer/deserializer (HSS) link pairs, a frequency offset can occur between the frequency of the data coming in and the reference clock. Any frequency offset between the transmitter and receiver of a link pair causes the clock-data-recovery (CDR) loop to chase the optimum sampling point with some delay. The inability to track the offset accurately increases jitter and degrades the link performance, e.g., by increasing the bit error rate.

Accordingly, a need exists for better compensation of frequency offset adjustment in a serial link transmitter/receiver pair. The present invention addresses such a need.

SUMMARY OF THE INVENTION

Aspects of providing automatic adaptation to frequency offsets in high speed serial links are described. First signals for phase adjusts in a receiver link are adjusted by detecting trends in the first signals to generate second signals, the second signals improving a rate of compensation for the frequency offsets by the phase adjusts. An up/down counter is included for counting signals for phase adjustments by a clock-data-recovery loop of a serial receiver. An adder is coupled to the up/down counter and outputs accumulated data indicative of a trend in the phase adjustments. Combinatorial logic coupled to the adder adapts the signals based on the accumulated data.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a block diagram of an example embodiment of a phase rotator control adjustment circuit of logic components in accordance with the present invention.

Figure 2 illustrates a logic table for generating new rotate down (Rot_dn') and rotate up (Rot_up') signals by the circuit of Figure 1.

Figure 3 illustrates pseudo-code simulating the operation of a quarter-rate version of the circuit of Figure 1.

Figure 4 illustrates a block diagram of a receiver link including the circuit of Figure 1.

DETAILED DESCRIPTION

The present invention relates to providing automatic adaptation to frequency offsets in high speed serial links. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Typically, phase rotators are used to adjust the phase based on the frequency offset. The phase rotator receives a rotate up or rotate down signal based on early or late edge detections and then either rotates the phase up or rotates the phase down accordingly. The present invention monitors the rotate up and rotate down signal to determine how well the phase is being monitored. The monitoring information is used to predict a trend of movement in a particular direction by the circuit and cancel out the offset proactively based on the detected trend. Figure 1 illustrates a block diagram of an example embodiment of a phase rotator control adjustment circuit 8 of logic components to perform the monitoring in accordance with the present invention.

Referring now to Figure 1, rotate down (Rot_dn) and rotate up (Rot_up) signals from a phase rotator control (not shown) are input into an up/down counter 10. In a preferred embodiment, a chosen number of bits from the input signal are used for averaging, i.e., to determine how big a difference in the ups/downs is seen before the remaining bits of the input signal are added by an accumulator 12. In the example shown, 3 LSBs (least significant bits) of the received data are used for averaging, while 11 MSBs (most significant bits) are accumulated. The underflow and overflow states

of the accumulator 12 are input to combinatorial logic 14, along with the Rot_dn and Rot_up signals. From the combinatorial logic 14, new rotate down (Rot_dn') and rotate up (Rot_up') are generated, as indicated by the logic table of Figure 2.

Figure 3 illustrates pseudo-code simulating the operation of the circuit of Figure 1 for a quarter-rate version. As indicated, the process initiates by transforming the active circuitry for quarter-rate operation. A check is then made for early/late difference with a corresponding step in the counter of up or down. The counter data is averaged over the LSBs and the counter MSBs are added to the accumulator. A check of the overflow/underflow status of the accumulator and the rotate up and down signals occurs, as indicated, to generate the new rotate up and down signals as desired. In this manner, the overflow and underflow signals of the accumulator trigger 'blind' phase steps at a constant rate; the rate increases until the up and down inputs are balanced.

It should be appreciated that the operations of the receiver link occur as is standardly understood with a phase rotator that compensates for frequency offset. However, the resultant Rot_up' and Rot_dn' signals from the phase rotator adjustment circuitry of the present invention reduces jitter and allows handling of much larger offsets when implemented in a receiver link, such as that shown in Figure 4. Referring to Figure 4, a differential signal is received in a receiver 20 that passes the data to latches 22 and 24 and then to memory 26. The data from memory 26 is output to a shift register 28 that is coupled to a rate counter 30 and 8/10 bit register 32. The memory 26 is further coupled to XOR (exclusive-OR) logic 34, which is used to generate early and late signals for a phase rotator control 36. The Rot_up and Rot_dn signals from the phase rotator control 36 are passed to an OR gate 38 and to the phase rotator control adjustment circuit 8. The OR gate 38 logically combines the Rot_up and Rot_dn signal from control 36 with the Rot_up' and Rot_dn' from adjustment circuit 8

of the present invention as presented hereinabove and outputs the result to a phase rotator counter 40. As is commonly understood, the counter 40 data passes through a thermometer code generator 42 and latches 44 before being received by a phase rotator 46. A multi-phase half-rate PLL (phase-locked loop) 48 is also coupled to the phase rotator 46. The data from the phase rotator 46 produces a logic clock signal and is fed back to the latches 22, as shown.

Thus, with the inclusion of the present invention in an HSS link, a straightforward enhancement of serial links is achieved that provides an efficient and effective manner of better compensating for frequency offsets. Further, by monitoring the long term trends of phase adjusts created by the clock and data recovery circuit of the serial link, better adaptation of the phase adjustment occurs through creation of future adjusts based on the previous adjusts.

From the foregoing, it will be observed that numerous variations and modifications may be effected without departing from the spirit and scope of the novel concept of the invention. It is to be understood that no limitation with respect to the specific methods and apparatus illustrated herein is intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.